3. A memory array comprising

a plurality of floating gate transistors connected in series,

each floating gate transistor having formed, in a well of a substrate,

a source and a drain region

and

a channel region separating said source and drain regions, said channel region having a non-uniform concentration of dopant;

wherein said non-uniform concentration comprises a retrograde concentration distribution in the direction from the surface of the substrate,

and wherein said non-uniform concentration comprises a lateral concentration distribution along the length of the channel that is higher in a region generally towards the central portion of the channel region and decreases toward the opposing source and drain regions.

4. The memory array of claim 3 wherein the non-uniform concentration is formed by a tilted ion implantation utilizing as a mask a gate structure of each floating gate transistor.

9. A transistor comprising,

in a well structure of a substrate, a source and a drain region and a channel region separating the source and the drain region, said channel region having a non-uniform concentration of dopant,

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wherein said non-uniform concentration comprises a retrograde concentration distribution in the direction away from the surface of the substrate,

and wherein said non-uniform concentration comprises a lateral concentration distribution along the length of the channel that is higher in a region generally towards the central portion of the channel region and decreases toward the opposing source and drain regions.

12. The transistor of claim 9 wherein

said non-uniform distribution is provided by a tilted ion implantation utilizing as a mask at least part of a gate structure of said transistor.

13. The transistor of claim 9, wherein the transistor is an NMOS transistor.

14. The NMOS transistor of claim 13, wherein the NMOS transistor is a floating gate transistor.

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